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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/696,580	10/30/2003	Shuichi Takahashi	492322014400	7212

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MORRISON & FOERSTER LLP
1650 TYSONS BOULEVARD
SUITE 300
MCLEAN, VA 22102

EXAMINER	
NGUYEN, DAO H	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 03/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/696,580	TAKAHASHI ET AL.	
	Examiner	Art Unit	
	Dao H. Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1205*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In response to the communications dated 12/27/2005, claims 1-8 are active in this application.

Acknowledges

2. Receipt is acknowledged of the following items from the Applicant.

Information Disclosure Statement (IDS) filed on 12/27/2005. The references cited on the PTOL 1449 form have been considered.

Remarks

3. Applicant's argument(s), filed 12/27/2005, with respect to claims 1-8 have been fully considered. With regard to the argument(s) relating to the teachings of Mochizuki et al., they are persuasive. Therefore, corresponding rejection(s) has/have been withdrawn.

However, with regard to the argument(s) relating to the teachings of Ishida, Examiner do/does not agree with Applicant's argument(s) that Ishida does not disclose the device wherein some but not all of the memory transistors are connected with corresponding bit lines by corresponding metal plugs of the one of the insulating layers; that all of the memory transistors of Ishida are connected to corresponding bit lines.

As shown in figs. 8C and/or 17C, the device of Ishida comprising three (3) transistors, which respectively having word line 1 (WL1), word line 2 (WL2), and gate line 2 (GL2). The transistor having GL2 includes two contact pads; one of which is connected to the ground (VSS), and the other of which is connected to the storage node interconnection (30b). This transistor (GL2) is clearly not connected to the bit line.

For the above reason(s), it is believed that Ishida does teach the claimed device wherein some but not all of the memory transistors are connected with corresponding bit lines by corresponding metal plugs of the one of the insulating layers. Therefore, the previous rejection should be retained, and further rewritten as following, in responding to the amendment(s).

In addition, newly discovered reference to Amanuma (U.S. Patent No. 6,316,801) is also used and combined with the reference to Ishida to make rejections to claims 3, 4, 7, and 8.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claim(s) 1, and 5-6 are rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 6,537,877 to Ishida.

Regarding claim 1, Ishida discloses a nonvolatile semiconductor memory device, as shown in figs. 1, 8c, comprising:

a plurality of memory transistors;

a plurality of insulating layers 20, 32, 38 (fig. 8c) disposed over the transistors;

a plurality of metal layers 31a, 36a, BL1, each of the metal layers 31a, 36a, BL1 being disposed on one of the insulating layers 20, 32, 38; and

a plurality of metal plugs 22a, 34a, 39a disposed over corresponding memory transistors, each of the metal plugs 22a, 34a, 39a filling in a contact hole formed in one of the insulating layers and electrically connecting the metal layers disposed on a top side and a bottom side of the corresponding insulating layer,

wherein a top metal layer BL1 of the plurality of metal layers is configured to provide bit lines that correspond to the memory transistors, the metal plugs 22a, 34a, 39a are vertically aligned, and one of the insulating layers (layer 38) is configured so that one of the memory transistors is connected to a corresponding bit line BL1 when a metal plug 39a corresponding to said one of the memory transistors is provided in said one of the insulating layers.

Regarding claim 2, Ishida discloses the nonvolatile semiconductor memory device wherein the insulating layer 32 (fig. 7C), 38 (fig. 16C) configured for memory transistor connection is a top insulating layer of the plurality of the insulating layers.

Regarding claim 5, Ishida discloses a nonvolatile semiconductor memory device, as shown in figs. 1, 8c, comprising:

a plurality memory transistors;

a first insulating layer 20 disposed on the memory transistors;

a plurality of first metal plugs 22a filling in contact holes formed in the first insulating layer 20, each of the memory transistors being connected to one of the first metal plugs 22a;

a first metal layer 31a disposed on the first metal plugs 22a;

a second insulating layer 32 disposed on the first metal layer 31a;

a plurality of second metal plugs 34a filling in contact holes formed in the second insulating layer 32, each of the first metal plugs 22a being connected to one of the second metal plugs 34a through the first metal layer 31a;

a second metal layer 36a disposed on the second metal plugs 34a;

a third insulating layer 38 disposed on the second metal layer 36a; and

a third metal layer BL1 disposed on the third insulating layer 38 and providing bit lines, wherein a plurality of third metal plugs 39a filling in contact holes formed in the third insulating layer 38 are arranged so that one of the memory transistors is connected to a corresponding bit line BL1 when a third metal plug 39a corresponding to said one of the memory transistors is provided in the third insulating layer 38, and the first metal plugs 22a, the second metal plugs 34a, the third metal plugs 39a, and

the memory transistors are vertically aligned for the memory transistors that have corresponding third metal plugs 39a.

Regarding claim 6, Ishida discloses a nonvolatile semiconductor memory device, as shown in figs. 1, 8c, comprising:

a plurality memory transistors;

a first insulating layer 20 disposed on the memory transistors;

a plurality of first metal plugs 22a filling in contact holes formed in the first insulating layer 20, each of the memory transistors being connected to one of the first metal plugs 22a;

a first metal layer 31a disposed on the first metal plugs 22a;

a second insulating layer 32 disposed on the first metal layer 31a;

a second metal layer 36a disposed on the second insulating layer 32;

a third insulating layer 38 disposed on the second metal layer 36a;

a plurality of third metal plugs 39a filling in contact holes formed in the third insulating layer 38, each of the third metal plugs 39a being disposed on one of the memory transistors; and

a third metal layer BL1 disposed on the third metal plugs 39a and providing bit lines,

wherein a plurality of second metal plugs 34a filling in contact holes formed in the second insulating layer 32 are arranged so that one of the memory transistors is connected to a corresponding bit line BL1 when a second metal plug 34a

corresponding to said one of the memory transistors is provided in the second insulating layer 32, and the first metal plugs 22a, the second metal plugs 34a, the third metal plugs 39a and the memory transistors are vertically aligned for the memory transistors that have corresponding second metal plugs.

Claim Rejections - 35 U.S.C. § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim(s) 3, 4, 7, and 8 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,537,877 to Ishida, in view of Amanuma (U.S. Patent No. 6,316,801).

Regarding claims 3, 4, 7, and 8, Ishida discloses the device comprising all claimed limitations, except for a size of the metal plugs filling in the contact holes in a top insulating layer of the plurality of insulating layers is larger than a size of the metal plugs filling in the contact holes in an insulating layer of the plurality of insulating layers that is not the top insulating layer; nor a size of the second metal plugs and a size of the third metal plugs are both larger than a size of the first metal plugs.

Amanuma discloses a memory device, as shown in figs. 2, 6, 9, 15, comprising plurality of metal plugs connecting to the transistors in/on the substrate 1; wherein a size of the metal plugs 12 filling in the contact holes in a top insulating layer 11 of the plurality of insulating layers (5, 8, 11) is larger than a size of the metal plugs 6 filling in the contact holes in an insulating layer 5 of the plurality of insulating layers that is not the top insulating layer; and/or wherein a size of the second metal plugs 9 and a size of the third metal plugs 12 are both larger than a size of the first metal plugs 6.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the sizes of the metal plugs of Ishida so that they would have sizes similar to those of Amanuma, since such modifications would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955). Moreover, it would have been well known to those skills in the art that a conductive plug with a larger in size would have less current resistance. Thus, it would be obvious that modifying the metal conductive plugs of Ishida to be similar to those of Amanuma would obtain the benefit of less current lost due to current resistance.

Conclusion

8. **THIS ACTION IS MADE FINAL.** A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday 9:00am - 6:00pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms, can be reached on (571)272-1787. The fax numbers for all communication(s) is (571)273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.

David Nelms
Supervisory Patent Examiner
Technology Center 2800

Dao H. Nguyen
Art Unit 2818
February 22, 2006